

General Description

The PT6112X is a high-efficiency synchronous Buck converter that can operate over a wide input voltage range of 2.5V to 5.5V and can deliver up to 2A of output current. It integrates the main switch and synchronous switch inside, and has extremely low on-resistance to reduce conduction loss. The switching frequency is 1.5MHz, which can reduce the size of the external inductor and output capacitor and reduce the output voltage ripple.

The PT6112M5/M6/F6 is available in SOT23-5 / SOT23-6 package.

Features

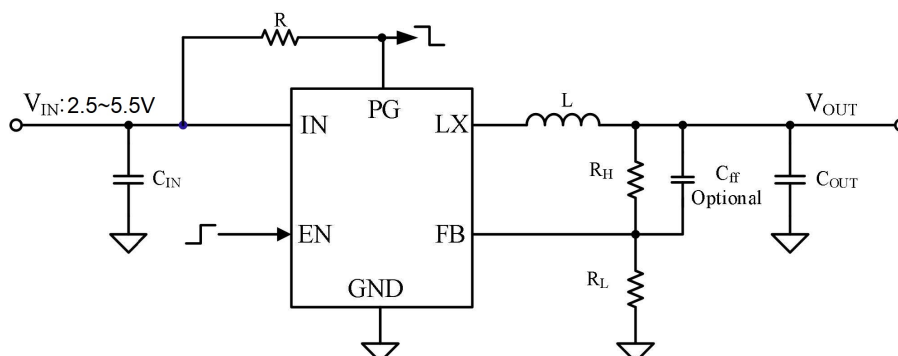
- 2.5V~5.5V input voltage range
- 35uA ultra-low quiescent current
- Internal soft-start reduces chip stress
- Input Overvoltage Protection (OVP)
- Short circuit protection Hiccup mode
- Internal integrated low $R_{DS(ON)}$ switch
- 1.5MHz switching frequency minimizes external components
- Optimized PFM mode for battery applications to improve light-load efficiency and extend battery life

- 100% duty cycle supports input and output low dropout operation
- RoHS Compliant and Halogen Free
- PT6112M5:SOT23-5 / PT6112M6:SOT23-6 package

Applications

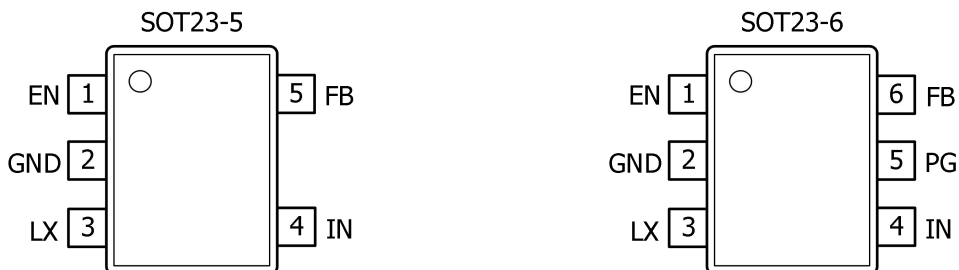
- Set-top box, security camera
- Mobile phones, handheld game consoles, media players
- Electric toys, meters, etc.

Typical Application Circuit



Power Good feature is only available in PT6112M6.

Pin Configurations



Pin Description

PIN		Symbol	Description
SOT23-5	SOT23-6		
1	1	EN	Enable signal input pin, the chip works when input high level, do not leave the pin floating.
2	2	GND	Ground pin.
3	3	LX	Inductor pin. This pin should be connected to the switching node of the inductor.
4	4	IN	Power input pin. Use a ceramic decoupling capacitor of at least 4.7uF to connect this pin to ground.
-	5	PG	Power good pin, indicating whether the output power is ready.
5	6	FB	Feedback pin. Connect this pin to the center point of the output divider resistor to set the output voltage.

Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$)

Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	IN Pin Voltage Range to GND	-0.3	6.5	V
V_{LX}	LX Pin Voltage Range to GND	-0.3	6.5	V
V_{EN}, V_{FB}, V_{PG}	EN, FB, PG Voltage	-0.3	6.5	V
T_{STG}	Storage Junction Temperature	-55	150	$^{\circ}\text{C}$
T_A	Operating Temperature Range	-40	85	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance, Junction to Ambient	-	170	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance, Junction to Case	-	130	$^{\circ}\text{C}/\text{W}$
ESD	Electrostatic Discharge Capability Human Body Model, ANSI/ESDA/JEDEC JS-001-2017		2	kV
	Electrostatic Discharge Capability Charged Device Model, ANSI/ESDA/JEDEC JS-002-2018		1	kV

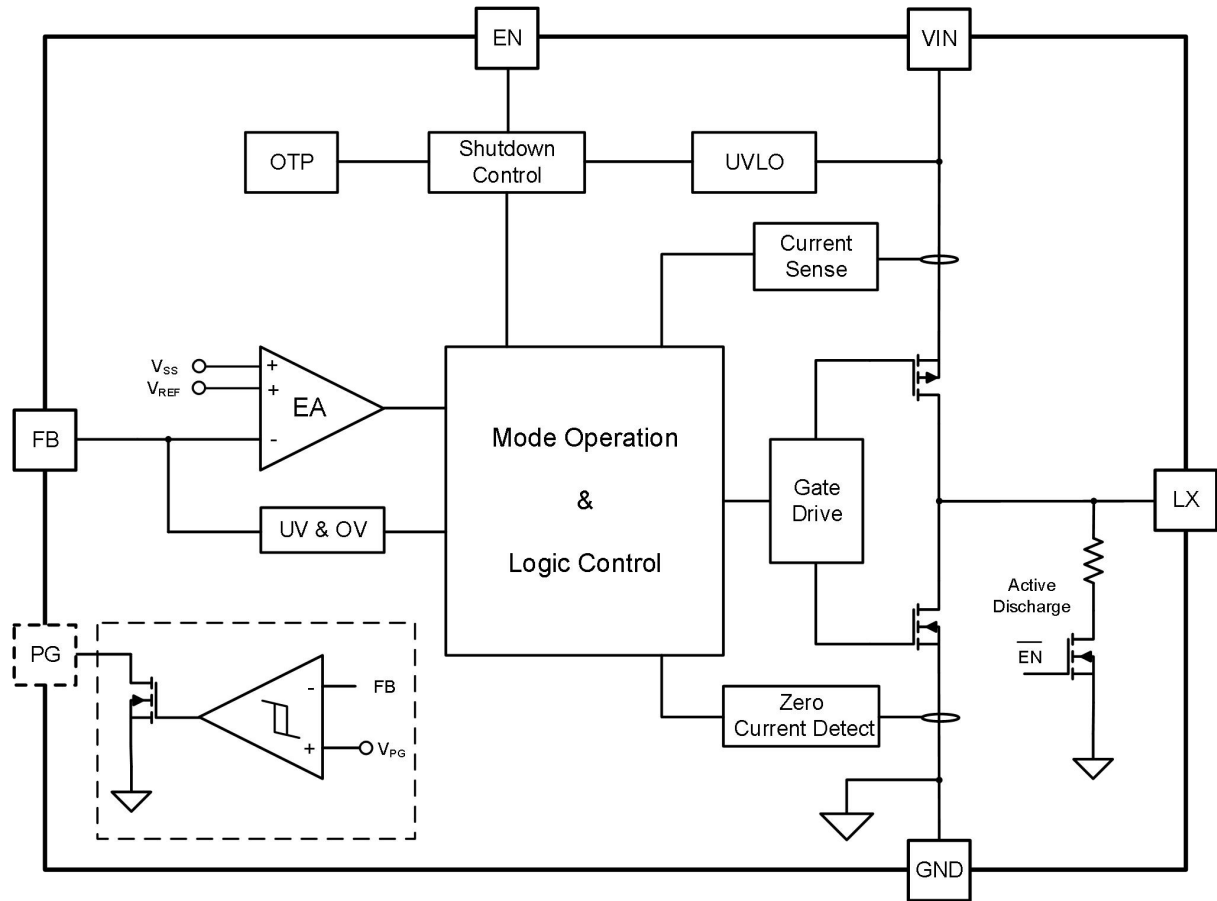
Electrical Characteristics (T_A=25°C)

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2uH, C_{OUT} = 22uF, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{IN}	Input Voltage Range	-	2.5		5.5	V
V _{UVLO}	Input UVLO threshold	V _{IN} rising		2.3	2.45	V
V _{HYS}	UVLO hysteresis			0.18		V
OVP	VIN OVP Threshold	V _{IN} rising		6.2		V
I _Q	Quiescent Current	I _{OUT} =0, V _{FB} =V _{REF} *105%		35	65	μA
I _{SHDN}	Shutdown Current	V _{EN} =0V		0.1	10	μA
V _{REF}	Feedback Reference Voltage		0.588	0.600	0.612	V
R _{DS(ON),P}	PFET RON			115		mΩ
R _{DS(ON),N}	NFET RON			60		mΩ
I _{LIM}	PFET Current Limit	V _{OUT} =2.5V	3			A
R _{Dis}	LX Discharge Resistance	V _{EN} =0V		50		Ω
V _{ENH}	EN rising threshold	-	1.5			V
V _{ENL}	EN falling threshold	-			0.4	V
I _{EN_LK}	EN Leakage Current			0.01	1.0	uA
V _{PG_TH}	Power Good Threshold	PG low, FB falling PT6112M6		90		%
		PG high, FB rising PT6112M6		90		%
I _{PG_SINK}	Power Good Sink Current	PT6112M6			2	mA
F _{OSC}	Oscillator Frequency	I _{OUT} =1A		1.5		MHz
		V _{OUT} =0V		400		kHz

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _{ON_MIN}	Min ON Time			60		ns
D _{MAX}	Max Duty Cycle		100			%
T _{SS}	Soft Start Time			500		us
T _{SD}	Thermal Shutdown Temperature			165		°C
T _{HYS}	Thermal Shutdown Hysteresis			25		°C

Block Diagram

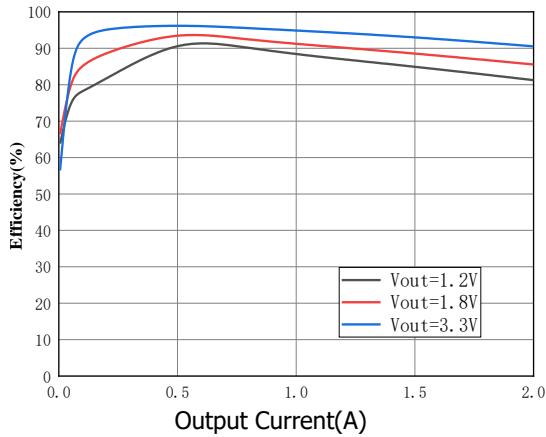


Power Good feature is only available in PT6112M6.

Typical Performance Characteristics

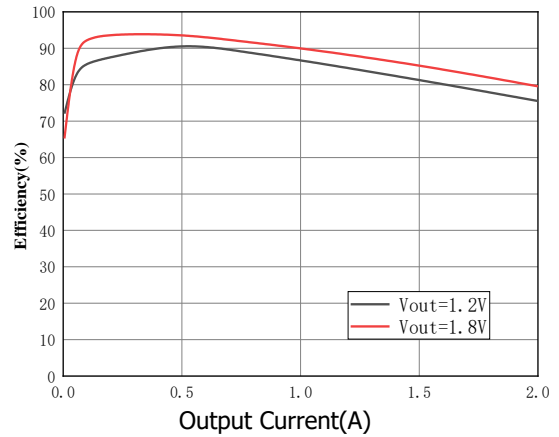
Efficiency vs. Output Current

($V_{IN}=5V$, $C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$)



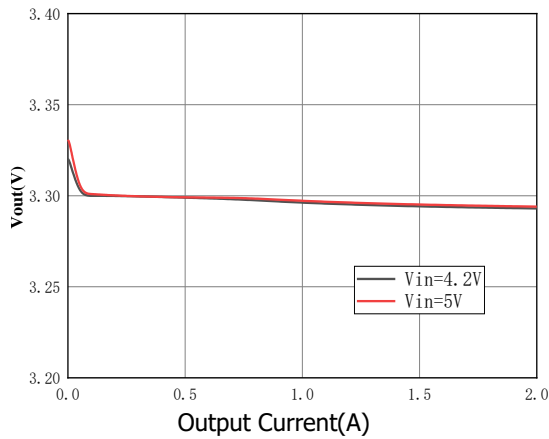
Efficiency vs. Output Current

($V_{IN}=3.3V$, $C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$)



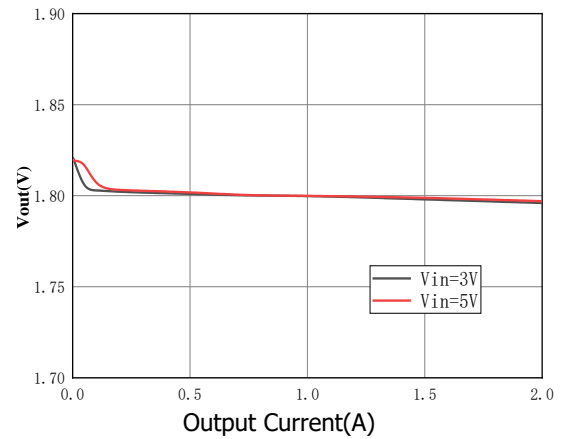
Output Voltage vs. Output Current

($V_{OUT}=3.3V$, $C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$)



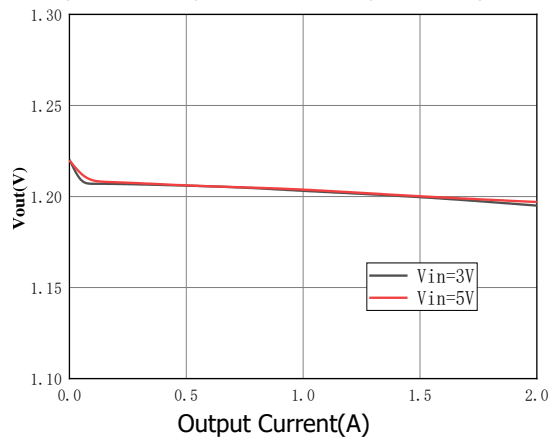
Output Voltage vs. Output Current

($V_{OUT}=1.8V$, $C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$)



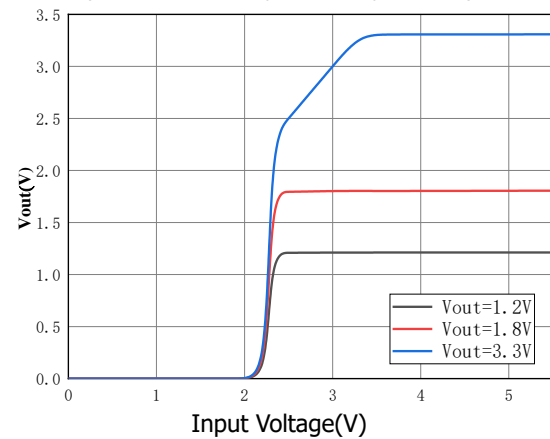
Output Voltage vs. Output Current

($V_{OUT}=1.2V$, $C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$)



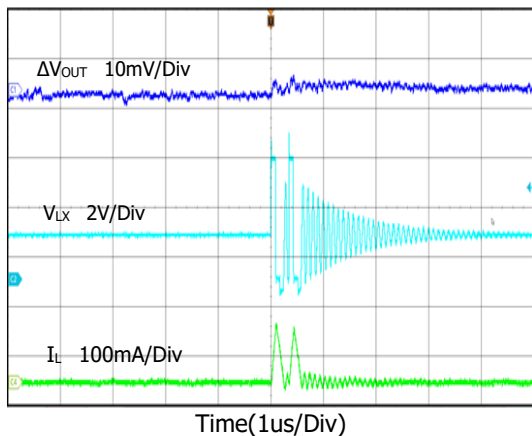
Input Voltage vs. Output Voltage

($C_{IN}=C_{OUT}=22\mu F$, $L=2.2\mu H$, $I_{OUT}=0A$)



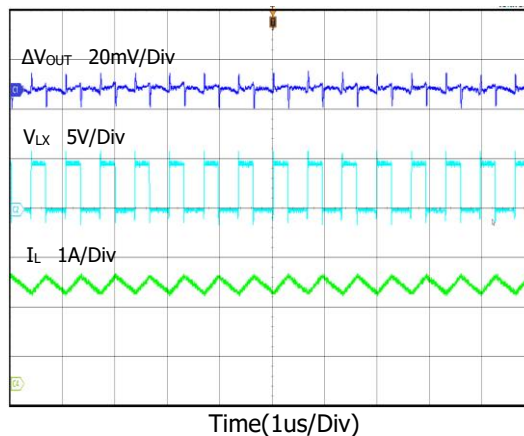
Output Ripple

($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0A$)



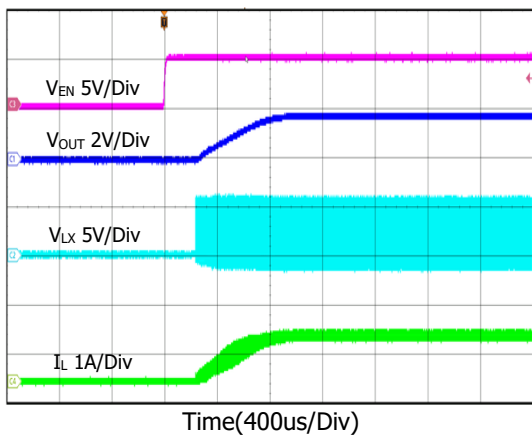
Output Ripple

($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{OUT}=2A$)



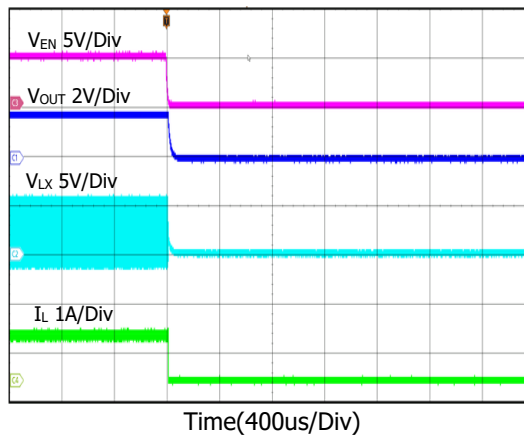
Startup from Enable

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_L=0.9\Omega$)



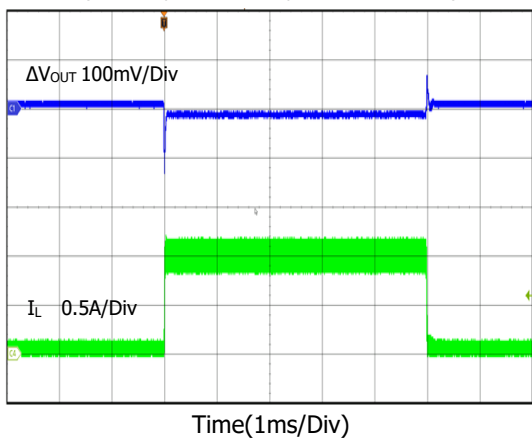
Shutdown from Enable

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_L=0.9\Omega$)



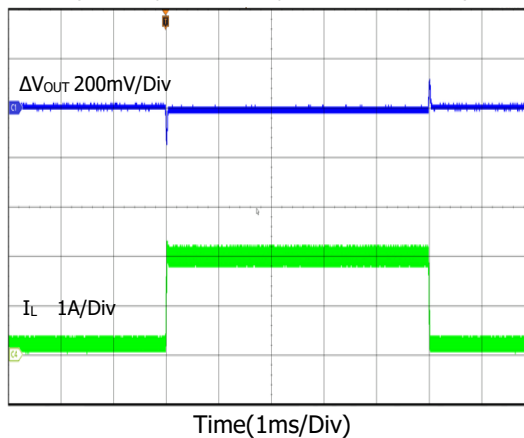
Load Transient

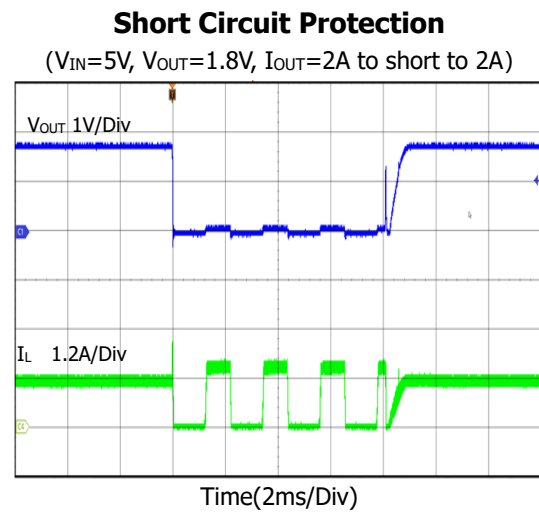
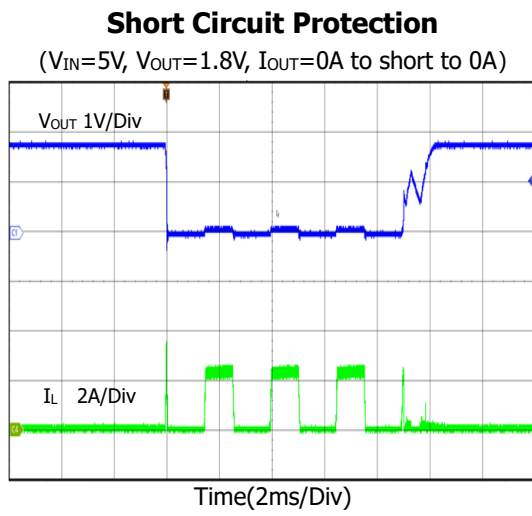
($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0A$ to $1A$)



Load Transient

($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{OUT}=0.2A$ to $2A$)





Functional Description

1. Input Protection

The chip has an under-voltage lockout function, which ensures that the chip will not start until the battery voltage reach the specified voltage, and a hysteresis function is set for UVLO to ensure that noise on the power supply does not cause system failure. When the input voltage is less than 2.5V, the chip stops working and is in a protection state. The under-voltage lockout circuit of the chip has a simple structure, low power consumption, and only a very small static power consumption, which does not affect the efficiency of the power supply, hardly increases the burden on the chip cooling system and affects the stability of the system, and enables the system to be able to work properly.

2. Output Protection

The chip has an output over-voltage protection function, which prevents the power supply from inputting too high voltage to the more sensitive devices. Once the power has been switched on, the OVP will continue to working and cannot be switched off manually. If the output voltage exceeds the OVP setting value, the power output will be switched off, thus protecting the device from damage caused by excessive voltage.

The chip has an output over-current protection function, which prevents the load from being burned out due to excessive output current. When the output current exceeds the OCP setting value, the power supply output will be switched off.

The chip has a short-circuit protection function. When the output terminal is short-circuited, the chip will be switched off and the output will be stopped to avoid circuit damage.

3. Soft Start

During the power-up of the chip, the output voltage rises from zero to the maximum value. Due to the effect of negative feedback, the duty cycle of the PWM control signal of the power tube changes from the maximum value and gradually decreases until the circuit is stable. Due to the existence of output filter capacitors in the circuit, it is easy to generate inrush current when charging the capacitors. At this time, a large current will flow through the power tube, which is easy to burn the circuit system. Therefore, there is a voltage soft start in the chip, and the output voltage gradually increases from 0V to the rated output voltage during power-on, reducing the inrush current received by the load.

4. Power Good (only for PT6112M6)

The PG pin is an open-drain output state. When the chip is just powered on, the PG pin is in a high-impedance output state. When the output voltage is normal, the PG pin is a low impedance output. Connect a pull-up resistor to this pin to output a high level just after power-on, and output a low level after the output is stable.

5. FB Adjustment

FB is feed-back, the output voltage is divided by the resistor and then connected to this pin. The feedback voltage will be connected to the internal comparator of the chip and compared with the internal reference voltage(0.6V). The result of the comparison will control the change of the duty cycle, so as to achieve the purpose of stabilizing the voltage.

6. PWM/PFM Working Mode

The PWM/PFM hybrid control method is to stabilize the output voltage by changing the width and pulse frequency of the square wave. At full load, PWM is used, which has relatively high efficiency and a wide range of duty cycles. The PFM work mode is used at light load, which has higher efficiency than PWM.

Application Information

1. Setting the Output Voltage

The output voltage is set by an external resistor divider according to Equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_H}{R_L}\right) = 0.6V \times \left(1 + \frac{R_H}{R_L}\right)$$

There is no strict requirement for the feedback resistor. An R_H value greater than 10kΩ is reasonable for most applications. R_L must not be higher than 100 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

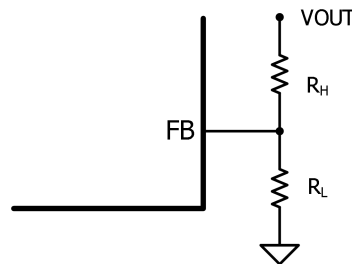


Figure 1 Feedback Network

2. Selecting the Inductor

Most applications work best with a 1 - 2.2μH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency. a high-frequency, switch-mode power supply with a magnetic device produces a strong electronic magnetic inference in the system. Any shield inductor, are ideal for applications as they can decrease the influence effectively.

For most designs, estimate the inductance value with Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_s}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

3. Selecting the Input Capacitor

A typical X5R or better grade ceramic capacitor with 6.3V rating and no less than 10μF capacitance is recommended. To minimize the potential noise problem, we place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

4. Selecting the Output Capacitor

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Estimate the output voltage ripple with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and no less than 10μF capacitance.

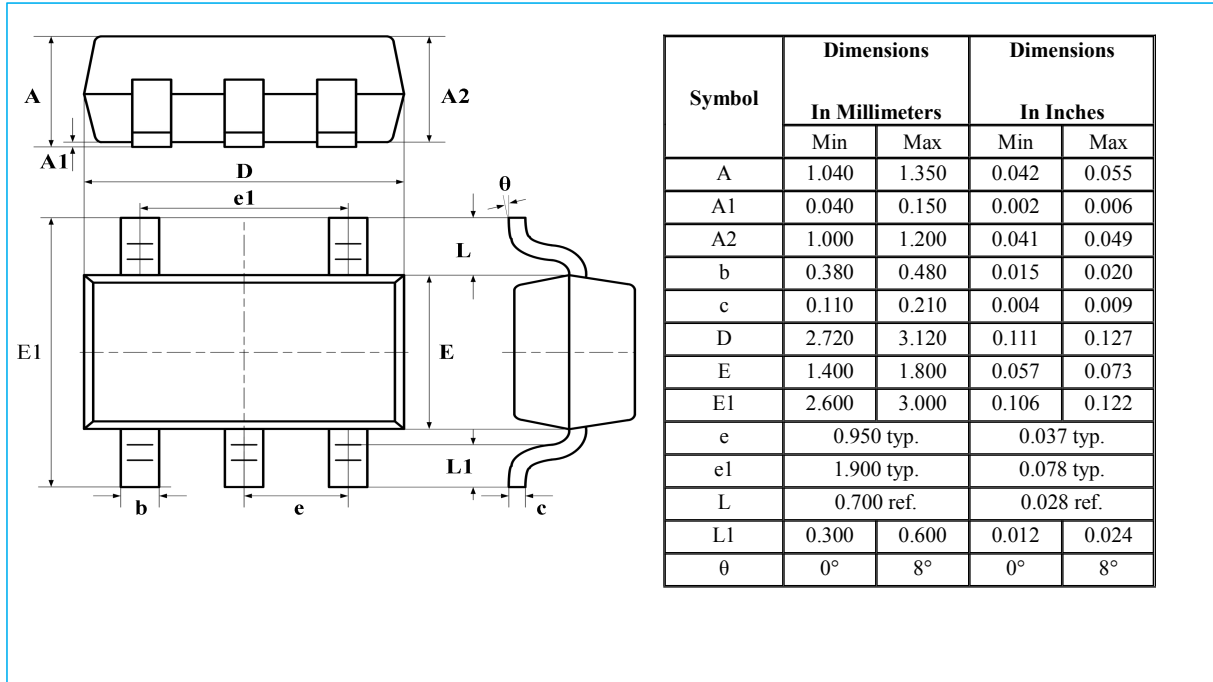
5. PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For best results, follow the guidelines below.

1. Place the high-current paths (GND, IN, and LX) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to IN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node LX short and away from the feedback network.
5. Keep the VOUT sense line as short as possible or away from the power inductor, especially the surrounding inductor.

Package Information

SOT23-5



SOT23-6

